

CLAIMS:

What is claimed is:

- 1 1. A method of processing power mode instruction, comprising:  
2       fetching and decoding a power mode instruction; and  
3       executing the power mode instruction on a combination of a CPU clock source and  
4 a peripheral clock source, wherein the power mode instruction initiates a switch to a clock  
5 source configuration associated with a literal  
6
- 1 2. The method according to claim 1, wherein the power mode instruction is a first power  
2 mode instruction.
- 1 3. The method according to claim 2, wherein the clock source configuration for the first  
2 power mode instruction corresponds to the CPU clock source and the peripheral clock  
3 source derived from a primary oscillator.  
4
- 1 4. The method according to claim 1, wherein the power mode instruction is a second  
2 power mode instruction.  
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- 1 5. The method according to claim 4, wherein the clock source configuration for the  
2 second power mode instruction corresponds to the CPU clock source and the peripheral  
3 clock source derived from a low power internal RC.

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1 6. The method according to claim 1, wherein the power mode instruction is a third power  
2 mode instruction.

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1 7. The method according to claim 6, wherein the clock source configuration for the  
2 second power mode instruction corresponds to the CPU clock source and the peripheral  
3 clock source derived from a secondary oscillator.

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1 8. The method according to claim 1, wherein the power mode instruction is a fourth  
2 power mode instruction.

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1 9. The method according to claim 8, wherein the clock source configuration for the  
2 second power mode instruction corresponds to disabling the CPU clock source and the  
3 peripheral clock source.

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1 10. The method according to claim 1, wherein the power mode instruction is a fifth power  
2 mode instruction.

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1 11. The method according to claim 10, wherein the clock source configuration for the  
2 second power mode instruction corresponds to disabling the CPU clock source and  
3 deriving the peripheral clock source from a low power internal RC.

1 12. The method according to claim 1, wherein the power mode instruction is a sixth power  
2 mode instruction.

1 13. The method according to claim 1, wherein the clock source configuration for the  
2 second power mode instruction corresponds to disabling the CPU clock source and  
3 deriving the peripheral clock source from a secondary oscillator.

1 14. The method according to claim 1, further comprising:  
2 detecting that an interrupt condition has occurred.

1 15. The method according to claim 14, further comprising:  
2 loading an instruction immediately following the power mode instruction into an  
3 instruction register for execution.

1 16. The method according to claim 14, further comprising:  
2 loading the first instruction in an interrupt service routine for the interrupt into an  
3 instruction register for execution.

1 17. The method according to claim 14, further comprising:  
2 determining whether to service an interrupt associated with the interrupt condition  
3 based on CPU priority.

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1 18. A processor for performing a power mode instruction, comprising:

2 a program memory for storing instructions including a shadow register array

3 control instruction;

4 a program counter for identifying current instructions for processing; and

5 a clock transition logic for executing the power mode instruction on a combination

6 of a CPU clock source and a peripheral clock source, wherein the power mode instruction

7 initiates a switch to a clock source configuration associated with a literal

1 19. The processor according to claim 18, wherein the power mode instruction is a first

2 power mode instruction.

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1 20. The processor according to claim 19, wherein the clock source configuration for the

2 first power mode instruction corresponds to the CPU clock source and the peripheral

3 clock source derived from a primary oscillator.

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1 21. The processor according to claim 18, wherein the power mode instruction is a second

2 power mode instruction.

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1 22. The processor according to claim 21, wherein the clock source configuration for the  
2 second power mode instruction corresponds to the CPU clock source and the peripheral  
3 clock source derived from a low power internal RC.  
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1 23. The processor according to claim 18, wherein the power mode instruction is a third  
2 power mode instruction.  
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1 24. The processor according to claim 23, wherein the clock source configuration for the  
2 second power mode instruction corresponds to the CPU clock source and the peripheral  
3 clock source derived from a secondary oscillator.  
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1 25. The processor according to claim 18, wherein the power mode instruction is a fourth  
2 power mode instruction.  
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1 26. The processor according to claim 25, wherein the clock source configuration for the  
2 second power mode instruction corresponds to disabling the CPU clock source and the  
3 peripheral clock source.

1 27. The processor according to claim 18, wherein the power mode instruction is a fifth  
2 power mode instruction.  
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4 28. The processor according to claim 27, wherein the clock source configuration for the  
5 second power mode instruction corresponds to disabling the CPU clock source and  
6 deriving the peripheral clock source from a low power internal RC.

7  
1 29. The processor according to claim 18, wherein the power mode instruction is a sixth  
2 power mode instruction.

1 30. The processor according to claim 29, wherein the clock source configuration for the  
2 second power mode instruction corresponds to disabling the CPU clock source and  
3 deriving the peripheral clock source from a secondary oscillator.

1 31. The processor according to claim 18, further comprising:  
2 interrupt logic for detecting that an interrupt condition has occurred.

1 32. The processor according to claim 31, further comprising:  
2 an instruction register for loading an instruction immediately following the power  
3 mode instruction into an instruction register for execution interrupt service routine (ISR)  
4 for an interrupt servicing the interrupt condition.

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1 .33. The processor according to claim 31, further comprising:

an instruction register for loading the first instruction in an interrupt service routine  
for the interrupt into an instruction register for execution.

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